UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,350	11/25/2003	Jagrut V. Patel	030217	4737

7590 03/21/2007

QUALCOMM Incorporated
Attn: Patent Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
RAHMAN, FAHMIDA	
ART UNIT	PAPER NUMBER
2116	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,350	PATEL ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12 and 14-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-12, 14-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 1/25/2007.

2. Claims 1, 12, 23, 25 have been amended, claims 2 and 13 have been canceled.

Thus, claims 1, 3-12, 14-26 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3, 4, 5, 6, 10, 12, 14-17, 21, 23-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Schaefer (US Patent 6930949).

For claim 1, Schaefer teaches the following limitations:

An electronic device (Fig 1), **comprising:**

an electronic component (112 and DQ buffers 212a-212i));

and an integrated circuit (140, 122, 120, 124) **configured to generate a system clock** (CK 202) **and an external clock** ("CKLD", the output of 208 in Fig 2) **having a programmable delay from the system clock** (202 is delayed by 208, which is programmed by 206, to generate CKLD), **the integrated circuit being further**

configured to provide the external clock to the electronic component to support communications therewith, communicate with the electronic component (Fig 2 shows the clock CLKD is provided to DQ buffers. As DQ buffers are associated with output of memory, the external clock is provided to the electronic component to support the communications), **and calibrate the external clock delay as a function of the communications** (206 of Fig 2 shows the calibration of external clock delay as a function of communication), **wherein the communications comprise a plurality of transmissions between the integrated circuit and the electronic component** (signal propagation variations are adjusted continuously as mentioned in lines 50-55 of column 2. Therefore, plural transmissions are adjusted if necessary), **the integrated circuit being further configured to program a different external clock delay for each of the transmissions** (delay is programmed with respect to variations, therefore it is variable as mentioned in lines 30-40 of column 1), **to communicate each of the transmissions between the integrated circuit and the electronic component in response to the corresponding different external clock delays** (variations are adjusted to provide adjusted clock during data valid window as mentioned in lines 50-55 of column 2), **to record timing parameters associated with each of the transmissions communicated between the integrated circuit and the electronic component in response to the communication of each of the transmissions** (210 shows the feedback loop, i.e., in response to communication, which records the timing parameter A and B of current transmission), **and to calibrate the external clock delay as a function of the transmissions to support future communications between**

the integrated circuit and the electronic component (206 takes the old parameter driven input and provides output to 208 so that future communications can be performed properly).

For claim 3, 112 is a memory.

For claim 4, the output of 210 is feedback clock. As CLKD is generated from feedback clock, feedback clock is used to sample data read from memory. External clock CLKD is used for read/write operation (lines 34-36 of column 1 mention about data launch and data capture).

For claim 5, the system calibrates the feedback as feedback clock is produced from external clock.

For claim 6, lines 50-55 of column 2 mention that data launch (i.e., read) operations are performed with necessary delay adjustment, which include adjustment in external clock and feedback clock.

For claim 10, memory is a SDRAM (line 15 of column 1).

For claims 12, 14-17 and 21, the method recited corresponds to the system recited in claims 1, 3-6 and 10. Since the system recited in claim 12, 14-17 and 21 is configured

to perform the method recited in claims 1, 3-6 and 10, the cited prior art that teaches the limitations of claims 1, 3-6 and 10 also teaches claims 12, 14-17 and 21.

For claims 23 and 25, claim 23 recites the means necessary for the system recited in claim 1 and claim 25 recites the media embodying a program to perform the corresponding method of the system recited in claim 1. The means and media is required to implement the corresponding system and method. Thus, the cited prior art that teaches the limitations of claim 1 also teaches claims 23 and 25.

For claims 24 and 26, output of 210 is feedback clock that has a programmable delay from system clock as it is generated from CLKD and clock C in Fig 2, which is generated from CKLD, is used for read/write (i.e., data launch and data capture). As feedback clock is produced from external clock, it can be said that feedback clock is used to sample read data. The system calibrates CLKD and therefore, calibrates feedback clock.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent 6930949).

For claims 11 and 22, Schaefer does not teach any wireless telephone. However, Examiner takes an official notice that wireless telephone is well known in the art.

One ordinary skill in the art would have been motivated to incorporate the teachings of Schaefer into an wireless telephone system, since the system of Schaefer ensures the correct timing of memory in the digital electronic systems. Wireless telephone is digital electronic system that requires memory to store the information. Thus, the invention of Schaefer would be beneficial to the wireless system in maintaining the precision of timing of memory.

5. Claim 7, 8, 9, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer (US Patent 6930949), in view of Cao et al (US patent Application Publication 2003/0001634).

For claim 7, Schaefer does not teach that the fixed offset between external and feedback clocks is used to calibrate the delay.

Cao et al teach a system where fixed offset between two clocks is used to calibrate the delay (Fig 3 shows that the two clocks are inputted to 40 and the offset between them is used to calibrate the delay).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Schaefer and Cao et al. One ordinary skill in the art would have been motivated to calibrate the delay using the offset between two clocks, since that would provide the desired resolution of the delay.

For claim 8, [0029] of Cao et al mention that maximum and minimum delays are stored and used to select a delay to calibrate the new delay.

For claim 9, selecting the center value between lowest and highest delay is within the scope of ordinary skill in the art. One ordinary skill in the art would have been motivated to select the delay to ensure that the chip is not operating outside the range of max and min value.

Claims 18-20 recite the method corresponding to the system recited in claims 7-9. Since the system recited in claim 7-9 is configured to perform the method recited in claims 18-20, the rejections for 7-9 described above are sufficient to reject claims 18-20.

Response to Arguments

Applicant's arguments filed on 1/25/2007 are moot in view of new grounds of rejections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116

A. ELAMIN
PRIMARY EXAMINER